

Code: EC6T1

**III B.Tech-II Semester–Regular/Supplementary Examinations
March 2020**

**VLSI DESIGN
(ELECTRONICS & COMMUNICATION ENGINEERING)**

Duration: 3 hours

Max. Marks: 70

PART – A

Answer *all* the questions. All questions carry equal marks

11x 2 = 22 M

1.

- a) Explain briefly about enhancement mode transistor action.
- b) Draw the transfer characteristics of a CMOS inverter.
- c) Define fall time.
- d) What is sheet resistance?
- e) What is the difference between Switch Logic and Gate Logic?
- f) Mention any three scaling factors for device parameters.
- g) What is Semi custom design?
- h) What is FPGA?
- i) What is Stuck-at model?
- j) Compare CMOS and Bipolar transistor.
- k) List out the Chip Level Test Techniques.

PART – B

Answer any *THREE* questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Determine Pull-up to Pull-down ratio for an nMOS inverter driven by another nMOS inverter. 8 M
b) Explain a P-well process in a CMOS fabrication with suitable diagrams. 8 M
3. a) Tabulate the encoding scheme for a simple single metal nMOS process with respect to various layers. 8 M
b) Estimate the CMOS inverter delay. 8 M
4. a) Define and give the expressions for any four scaling factors of MOS device. 8 M
b) Realize a 2:1 MUX using transmission gates. 8 M
5. a) Design a Full Adder using PLA. 8 M
b) Explain about Gate Array Design. 8 M
6. a) Design Built-In-Self -Test (BIST) scheme for memories. 8 M
b) Explain the key concepts of Design for testability. 8 M